＊魏一勤副教授

所有發表期刊論文及研討會論文

Journal Papers:

1. **I-Chyn Wey**, You-Gang Chen, and An-Yeu (Andy) Wu, "Design and Analysis of Isolated Noise-Tolerant (INT) Technique in Dynamic CMOS Circuits," in *IEEE Transactions on Very Large Scale Integration Systems*, accepted 2008 (SCI & EI).
2. **I-Chyn Wey**, You-Gang Chen, Changhong Yu, Jie Chen, and An-Yeu (Andy) Wu, "Design and Implementation of Cost-Effective Probabilistically-Based Noise-Tolerant Circuits," Submitting to *IEEE Transactions on Very Large Scale Integration Systems* (SCI & EI).

Conference Papers:

1. **I-Chyn Wey**, Lung-Hao Chang, You-Gang Chen, Shih-Hung Chang, and An-Yeu (Andy) Wu, "A 2Gb/s High-Speed Scalable Shift-Register Based On-Chip Serial Communication Design for SoC Applications," in *Proc. of 2005 IEEE International Symposium on Circuits and Systems*(*ISCAS 2005*), Kobe, Japan, pp. 1074-1077, May 2005.
2. Chia-Tsun Wu, Wei Wang, **I-Chyn Wey**, and An-Yeu (Andy) Wu, "A Scalable DCO Design for Portable ADPLL Designs," in *Proc. of 2005 IEEE International Symposium on Circuits and Systems* (*ISCAS 2005*), Kobe, Japan, pp. 5449-5452, May 2005.
3. **I-Chyn Wey**, You-Gang Chen, Chia-Tsun Wu, Wei Wang, and An-Yeu (Andy) Wu, "A High-Speed Scalable Shift-Register Based On-Chip Serial Communication Design for SoC Applications," in *Proc. of 2005 IEEE Ph.D. Research in Microelectronics and Electronics* (*PRIME 2005*), Lausanne, Switzerland, July 2005.
4. Chia-Tsun Wu, Wei Wang, **I-Chyn Wey**, An-Yeu (Andy) Wu, "A Frequency Estimation Algorithm for ADPLL Designs with Two-Cycle Lock-in Time,"

in *Proc. of 2006 IEEE International Symposium on Circuits and Systems* (*ISCAS 2006*), Kos Island, Greece, pp. 4082-4085, May 2006.

5. Wei Wang, **I-Chyn Wey**, Chia-Tsun Wu, and An-Yeu (Andy) Wu, "A Portable All-Digital Pulsewidth Control Loop for SOC Applications", in *Proc. of 2006 IEEE International Symposium on Circuits and Systems* (*ISCAS 2006*), Kos Island, Greece, pp. 3165-3168, May 2006.
6. **I-Chyn Wey**, You-Gang Chen, Changhong Yu, Jie Chen and An-Yeu (Andy) Wu,"0.18μm Probabilistic-Based Noise-Tolerate Circuit Design and Implementation with 28.7dB Noise-Immunity Improvement", *in Proc. of IEEE Asian Solid-State Circuits Conference* (*A-SSCC 2006*), Hangzhou, China, pp. 291-294, Nov. 2006.
7. You-Gang Chen, **I-Chyn Wey**, and An-Yeu (Andy) Wu, "A New Noise-Tolerant Dynamic Circuit Design with Enhanced PDP Performance under Low SNR Environment", *in Proc. of IEEE Asian Solid-State Circuits Conference* (*A-SSCC 2006*), Hangzhou, China, pp. 295-298, Nov. 2006.
8. Jhao-Ji Ye, You-Gang Chen, **I-Chyn Wey**, and An-Yeu (Andy) Wu, "Low-Latency Quasi-Synchronous Transmission Technique for Multiple-Clock-Domain IP Modules," in *Proc. of 2007 IEEE International Symposium on Circuits and Systems (ISCAS 2007)*, New Orleans, USA, pp. 869-872, May 2007.
9. Huifei Rao, Jie Chen, Changhong Yu, Woon Tiong Ang, **I-Chyn Wey**, An-Yeu (Andy) Wu, Hong Zhao, "**Ensemble Dependent Matrix Methodology for Probabilistic-Based Fault-tolerant Nanoscale Circuit Design,**" in *Proc. of 2007 IEEE International Symposium on Circuits and Systems (ISCAS 2007)*, New Orleans, USA, pp. 1803-1806, May 2007.
10. Woon Tiong Ang, Hui Fei Rao, Changhong Yu, Jilin Liu, **I-Chyn Wey**, An-Yeu (Andy) Wu, Hong Zhao, Jie Chen, "**A clock-fault tolerant architecture and circuit for reliable nanoelectronics system,**"*In Proc. of 2007 nternational Conference on Design & Technology of Integrated*

Systems in Nanoscale Era (DTIS 2007), Rabat, Morocco, pp. 186-191, Sep. 2007.

11. Sung-Tze Wu, Chih-Hao Chao, **I-Chyn Wey**, and An-Yeu (Andy) Wu, "Dynamic Channel Flow Control of Networks-on-Chip Systems for High Buffer Efficiency," *in Proc. of 2007 IEEE Workshop on Signal Processing Systems (SiPS-2007)*, Shanghai, China, pp. 493-498, Oct. 2007.
12. **I-Chyn Wey**, You-Gang Chen, Changhong Yu, Jie Chen and An-Yeu (Andy) Wu, "A 0.13μm Hardware-Efficient Probabilistic-Based Noise-Tolerant Circuit Design and Implementation with 24.5dB Noise-Immunity Improvement," *in Proc. of 2007 IEEE Asian Solid-State Circuits Conf. (A-SSCC-2007)*, Jeju, Korea, pp. 295-298, Nov. 2007.
13. Huifei Rao, Jie Chen, Vicky H. Zhao, Woon Tiong Ang, **I-Chyn Wey** and An-Yeu (Andy) Wu, "An Efficient Methodology to Evaluate Nanoscale Circuit Fault-tolerance Performance based on Belief Propagation," *accepted by 2008 IEEE International Symposium on Circuits and Systems (ISCAS 2008)*, Seattle, USA, May 2007.