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所有發表期刊論文及研討會論文

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- [2] **Shao-Ku Kao**, Fu-Jen Hsieh (2013): A fast-locking PLL with all-digital lockedaid circuit, *International Journal of Electronics*, 100:2, 245-258,01 Jun 2012
- [3] **Shao-Ku Kao**, Bo-Jiun Chen, and Shen-Iuan Liu, "A 62.5-625MHz Anti-reset All-digital Delay-locked Loop", *IEEE Trans. Circuits and Systems- II: Express Briefs*, vol.54, July 2007.
- [4] **Shao-Ku Kao** and Shen-Iuan Liu, "All-digital Fast-locked Synchronous Duty Cycle Corrector", *IEEE Trans. Circuits and Systems- II: Express Briefs*, vol.53, Dec. 2006.
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- [6] You-Jen Wang, **Shao-Ku Kao**, and Shen-IuanLiu, "All-Digital Delay-Locked Loop/Pulsewidth-Control Loop With Adjustable Duty Cycles", *IEEE J. Solid-State Circuits*, vol. 41, June 2006.

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[1]Bo-Jiun Chen, **Shao-Ku Kao**, Shen-Juan Liu," An All-digital Duty Cycle Corrector",*VLSI Design, Automation and Test, 2006 International Symposium on*, April 2006