＊ 許炳堅講座教授

所有發表期刊論文

專書

(1)許炳堅，《數位時代的孫悟空》，引號文創工作室，ISBN 978-98692-92504，台灣半導體產業協會贊助發行，2016 年

(2)許炳堅、吳重雨、柯明道，《追求 21 世紀的金鑰匙》，交通大學出版社，ISBN 978-98682-99740，2007 年

(3) 吳重雨、許炳堅，《21 世紀現代教育之我見》，交通大學出版社，ISBN 986-81857-5-0，2006 年

(4)B. J. Sheu, M. Ismail, 主編,《Multimedia Technologies for Applications》, 666 pages, (ISBN 0-7803-1174-4) IEEE Press: New York, 1998.

(5)B. J. Sheu, M. Ismail, E. Sanchez-Sinencio, T. Wu, 主編,《Microsystems Technology for Multimedia Applications》, 720 pages, (ISBN 0-7803-1156-6) IEEE Press: New York, May 1995.

(6)B. J. Sheu, J. Choi,《Neural Information Processing and VLSI》, 556 pages, (ISBN 0-7923-9547-6) Kluwer Academic Publishers: Boston, MA, 1995.

(7) B. W. Lee, B. J. Sheu,《Hardware Annealing in Analog VLSI Neurocomputing》, 234 pages, (ISBN 0-7923-9132-2) Kluwer Academic Publishers: Boston, MA, 1991.

科技書的專章

(1) B. W. Lee, B. J. Sheu, <Design and Analysis of VLSI Neural Networks>, Chapter 8 in《Neural Networks for Signal Processing》, pp. 229-286, Editor: B. Kosko, (ISBN 0-13-617390-X) Prentice-Hall: Englewood Cliffs, NJ, 1992.

(2) J. Choi, B. J. Sheu, <Neural Information Processing>, Chapter 7 in《Analog VLSI for Signal and Information Processing》, pp. 311-357, Editors: M. Ismail, T. Fiez, (ISBN 0-07-032386-0) McGraw-Hill: Reading, MA, 1994.

(3) J. C. Chang, B. J. Sheu, <MOS Storage Circuits>, Chapter 12.5.4 in《Circuits and Filters Handbook》, Editor: W.-K. Chen, CRC Press & IEEE Press, 1995; & 2nd Edition, 2003.

(4) R. C. Chang, B. J. Sheu, <Transmission Gates>, Chapter 12.4.2 in《Circuits and Filters Handbook》, Editor: W.-K. Chen, CRC Press & IEEE Press, 1995, & 2nd Edition, 2003.

(5) B. J. Sheu, E. Chou, R. Tsai, D. Chen,<VLSI Neural Networks: Design Challenges and Opportunities>, Chapter 19, pp. 261-273,《Computational Intelligence》, Editors: M. Palaniswami, Y. Attikiouzel, R. J. Marks II, D. Fogel, T. Fukada, IEEE Press, 1995.

(6) T. H. Wu, B. J. Sheu, <Simulated Annealing, Boltzmann Machine and Hardware Annealing>, Chapter 74 in《Industrial Electronics Handbook》, Editor: J. D. Irwin, (ISBN 0-8493-8343-9) CRC Press, 1997.

(7) Y. Oshima, B. J. Sheu, S. H. Jen, <DRAM Chips>, in《Encyclopedia of Electrical and Electronics Engineering》, Editor: J. Webster, Wiley & Sons Inc., 1998.

(8) T. W. Berger, R. D. Brinton, V. Z. Marmarelis, B. J. Sheu, A. R. Tanguay, <Brain-Implantable Biomimetic Electronics as a Neural Prosthesis for Hippocampal Memory Function>, Chapter 12 in 《Toward Replacement Parts for the Brain》, Editors: T. W. Berger, D. L. Glanzman, (ISBN 0-262-02577-9), MIT Press, 2005.

學術期刊：12 篇代表著作（總數超過 70 篇）

(1) B. J. Sheu, D. L. Scharfetter, P. K. Ko, M.-C. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistors," IEEE Journal of Solid- State Circuits, vol. SC-22, no. 4, pp. 558-566, Aug. 1987. (also included in《Digital MOS Integrated Circuits II》, Editor: Elmasry, pp. 101-108, IEEE Press, 1991).

(2) B. J. Sheu, C. Hu, "Switch-induced error voltage on a switched capacitor," IEEE Journal of Solid-State Circuits, vol. SC-19, no. 4, pp. 519-525, Aug. 1984.

(3) B. J. Sheu, P. K. Ko, "Measurement and modeling of short-channel MOS transistor gate capacitances," IEEE Journal of Solid-State Circuits, vol. SC-22, no. 3, pp. 464-472, Jun. 1987.

(4) B. J. Sheu, A. H. Fung, Y.-N. Lai, "A knowledge-based approach to analog integrated circuit design" IEEE Transactions on Circuits and Systems, vol. CAS-35, no. 2, pp. 256-258, Feb. 1988.

(5) B. J. Sheu, W.-J. Hsu, B. W. Lee, "An integrated-circuit reliability circuit simulator - RELY," IEEE Journal of Solid-State Circuits, vol. SC-24, no. 2, pp. 473-477, Apr. 1989.

(6) B. W. Lee, B. J. Sheu, "Modified Hopfield neural networks for retrieving the optimal solution," IEEE Transactions on Neural Networks, vol. 2, no. 1, pp. 137-142, Jan. 1991.

(7) W.-C. Fang, B. J. Sheu, O. T.-C. Chen, J. Choi, "A VLSI neural processor for image data compression using self-organizing networks," IEEE Transactions on Neural Networks, vol. 3, no. 3, pp. 506-518, May 1992.

(8) B. W. Lee, B. J. Sheu, "Paralleled hardware annealing for optimal solutions on electronic neural networks," IEEE Transactions on Neural Networks, vol. 4, no. 4, pp. 588-599, July 1993.

(9) W.-C. Fang, C.-Y. Chang, B. J. Sheu, O. T.-C. Chen, J. C. Curlander, "VLSI systolic binary tree-searched vector quantizer for image compression," IEEE Transactions on VLSI Systems, vol. 2, no. 1, pp. 33-44, Mar. 1994.

(10) S. H. Bang, B. J. Sheu, "A neural network for detection of signals in communication," IEEE Transactions on Circuits and Systems I, vol. 43, no. 8, pp. 644-655, Aug. 1996.

(11) R. H. Tsai, B. J. Sheu, T. W. Berger, "A VLSI Neural Network Processor Based on Hippocampal Model," Journal of Analog ICs & Signal Processing, Kluwer Academic Publishers, vol. 15, pp. 201-203, 1998.

(12) T. W. Berger, M. Baudry, R. D. Brinton, J.-S. Liaw, V. Marmarelis, A. Y. Park, B. J. Sheu, A. R. Tanguay, “Brain-Implantable Biomimetic Electronics as the Next Era in Neural Prosthetics,” Proceedings of the IEEE, vol. 89, no. 7, pp. 993-1012, July 2001.