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所有發表期刊論文

1.

Y.-H. Chen; <u>C.-Y. Li</u>(*); L.-A. Lai, "Fine-tuning accuracy using conditional probability of the bottom sign-bit in Fixed-width Modified Booth Multiplier", Circuits, Systems and Signal Processing (CSSP), Accepted.

2.

<u>C.-Y. Li</u> and L.-Y. Deng, "A Class of Hardware-based PRNGs with Maximum Periods", Journal of the Chinese Statistical Association, vol. 55, pp. 145–159, 2017.

3.

<u>C.-Y. Li</u> and Bo-Xun Wu, "Zeroing of Power Supply Noise Sensitivity for Ring Oscillators Operating from 1 to 4 GHz", Microelectronics Journal, vol. 67, issue 9, pp. 128 - 134, 2017.

4.

A. P. S. Isabel, C.-H. Kao, R. K. Mahanty, Y.-C. Sermon Wu, <u>C.-Y. Li</u>, C.-Yu Lin, and C.-Fu Lin, "Sensing and structural properties of Ti-doped tin oxide (SnO2) membranefor bio-sensor applications", Ceramics International, vol. 43, issue 13, pp. 10386 - 10391, 2017.

5.

<u>C.-Y. Li</u>, "Fast Locking Adaptive PLL using Dual-Edge Phase-Frequency Detector", Microelectronics Journal, vol. 46, issue 12, pp. 1413 - 1419, 2015.

6.

<u>C.-Y. Li</u>, C.-L. Lee, M.-H. Hu, and H.-P. Chou, "A Fast Locking-in and Low Jitter PLL with a Process-Immune Locking-In Monitor", IEEE Trans. On Very Large Scale Integration (VLSI) Systems, vol. 22, issue 10, pp. 2216 - 2220, 2014.

7.

C.-Y. Li, Y.-H. Chen, T.-Y. Chang, L.-Y. Deng, and K. W. To, "Period Extension and Randomness Enhancement Using High-Throughput Reseeding-Mixing PRNG," IEEE Trans. On Very Large Scale Integration (VLSI) Systems, vol. 20, issue 2, pp. 385-389, 2012.

8.

<u>C.-Y. Li, Y.-H. Chen, T.-Y. Chang, and J.-N. Chen, "A Probabilistic Estimation Bias Circuit for Fixed-width Booth Multiplier and Its DCT Applications," IEEE Trans. on Circuits and Systems II: Express Brief, vol. 58, no. 4, pp. 215-219, Apr. 2011.</u>

9

Y.-H. Chen, <u>C.-Y. Li</u>, T.-Y. Chang, "Area-Effective and Power-Efficient Fixed-Width Booth MultipliersUsing Generalized Probabilistic Estimation Bias," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 1, issue 3, pp. 277-288, 2011.

10.

Y.-H. Chen, T.-Y. Chang, <u>C.-Y. Li,</u> "High Throughput DA-based DCT with High Accuracy Error-compensated Adder Tree," IEEE Trans. On Very Large Scale Integration (VLSI) Systems,

vol. 19, no. 4, pp. 709-714, Apr. 2011.

11.

<u>C.-Y. Li</u>, L.-Y. Deng, J.-J. H. Shiau, T.-Y. Chang, and H. H.-S. Lu, "High-Throughput and Long-Period Nonlinear PRNGs by Shuffle-Hiding Linear Generators", To be re-submitted to IEEE Trans. On VLSI.

1.